

FORM PTO-892 (REV. 2-92)				U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	SERIAL NO. <u>07/852,517</u>	GROUP ART UNIT <u>2508</u>	ATTACHMENT TO PAPER NUMBER	<u>7</u>
NOTICE OF REFERENCES CITED				APPLICANT(S) <u>YAMAZAKI et al.</u>				

U.S. PATENT DOCUMENTS

*	DOCUMENT NO.	DATE	NAME		CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
A	4 727 044	2-88	<u>YAMAZAKI et al</u>		257	52	
B	4 803 528	2-89	<u>PANKOVE</u>		257	912	
C	4 814 292	3-89	<u>SASAKI et al</u>		437	233	
D	5 036 373	7-91	<u>YAMAZAKI</u>		257	86	
E	5 108 843	4-92	<u>OHFUKA et al</u>		428	446	11-89
F							
G							
H							
I							
J							
K							

FOREIGN PATENT DOCUMENTS

*	DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHTS. DWG.	PP. SPEC.
L	57 10 267	1-82	JP	<u>SAKURA I</u>	257	66		
M	6 354 773	3-88	JP	<u>HOSOKAWA</u>	257	66		
N	1 286 463	11-89	JP	<u>ISHIHARA</u>	257	66		
O								
P								
Q								

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

R	<u>WOLF et al., "SILICON PROCESSING FOR THE VLSI ERA," VOL. 1, LATTICE PRESS, SUNSET BEACH, CALIFORNIA, PP. 19-21</u>						
S							
T							
U							

EXAMINER <u>m. Saadat</u>	DATE <u>3-5-93</u>	
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* A copy of this reference is not being furnished with this office action.
(See Manual of Patent Examining Procedure, section 707.05 (a).)